UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,240	02/06/2004	Soon-Kyun Shin	9862-000023/US	6620

30593 7590 03/29/2005

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,240	SHIN, SOON-KYUN	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-25* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 10-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Henry (US 20020008567).

As to claim 1, Henry discloses in figure 4 an apparatus for controlling a boosted voltage, comprising: a voltage generating circuit (S1-S4, CX) configured to generate a boosted voltage (Vout) from an input voltage (Vin) based on a control current (IS1), and a control circuit (132, 134, 124) configured to generate the control current based on the boosted voltage.

As to claim 2, figure 4 shows that the voltage generating circuit comprises: a capacitor (Cx), and a switching structure (S1-S4) configured to selectively store charges corresponding to the input voltage in the capacitor, and to selectively output the stored charges in conjunction with charges corresponding to the control current as the boosted voltage.

As to claim 3, figure 4 shows that the control circuit is configured to generate the control current based on a difference between the boosted voltage and a desired boosted voltage (Vref).

As to claim 4, figure 4 shows that the voltage generating circuit comprises: first, second, third and fourth switches (S1-S4), and a capacitor (Cx) configured to store charges corresponding to the input voltage while the first and third switches (S1, S3) are turned on, and outputting the boosted voltage while the second and fourth switches (S2, S4) are turned on.

As to claim 10, figure 4 shows that the control circuit is configured to generate the control current based on the boosted voltage and a desired boosted voltage (Vref).

As to claim 11, figure 4 shows that the control circuit is configured to generate the control current based on a difference between the boosted voltage and the desired boosted voltage.

As to claims 12 and 14, figure 4 shows that the control circuit comprises: a voltage divider (132, 134) configured to generate a divided voltage from the boosted voltage, a comparator or amplifier (124) configured to compare the divided voltage with a reference voltage (Vref); and a current generator (122) configured to generate the control current based on output of the comparator.

As to claims 13 and 15, figure 4 shows that the reference voltage represents a desired boosted voltage.

As to claim 16, figure 4 shows that the voltage controlled current source decreases the control current when the divided voltage is higher than the reference voltage, and increases the control current when the divided voltage is lower than the reference voltage.

Claims 17-25 recite a method having similar limitations of claims above. Therefore, they are rejected for the same reasons.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Ting et al. (USP 6198340).

As to claim 1, Ting discloses in figures 1C and 4 an apparatus for controlling a boosted voltage (circuits 48, 50 in figure 4), comprising: a voltage generating circuit (48) configured to

generate a boosted voltage from an input voltage (Vcc) based on a control current (output of 50), and a control circuit (50) configured to generate the control current based on the boosted voltage.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 5 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ting et al. (USP 6198340) in view of Myono (US 20020030534).

As to claim 4, Ting et al.'s figure 1C shows the voltage generating comprises: third and fourth switches (21, 26), and a capacitor (C2). Figure 1 fails to show the first and second switches. However, Myono's figure 1 shows a buffer circuit (CD1') for driving charge pump capacitor. It would have been obvious to one having ordinary skill in the art to use two buffer circuits having the same structure as Myono's buffer circuit for driving the Ting et al.'s capacitors C1 and C2 for the purpose of shaping or buffering signals B1 and B2. Thus, the modified Ting et al.'s figure 1C further shows a first and second switches (Myono's M1'(P) ad M1'(N)), the capacitor configured to store charges corresponding to the input voltage while the first and third switches (S1, S3) are turned on, and outputting the boosted voltage while the second and fourth switches (S2, S4) are turned on.

As to claim 5, the modified Ting et al.'s figure 1C shows that the voltage generating circuit further comprises a clock signal generator configured to generate first (output of Myono's INV1'), second (output of Myono's INV2') and third (B1 in Ting et al.'s figure 1C) clock

signals; a level shifter circuit (C1, 10, 20) configured to selectively change a level of the input voltage in response to the third clock signal to output a switching control signal (at node 11), and wherein the first and second switches are switched in response to first and second clock signals, and the third and fourth switches are switched in response to a switch control signal.

As to claim 7, the modified Ting et al.'s figure 1C fails to show the capacitor is MOS capacitor. However, it is notoriously well known that MOS capacitor is more compact than regular capacitor. Therefore, it would have been obvious to one having ordinary skill in the art to use MOS capacitor for Ting et al.'s capacitors C1, C2 for the purpose of saving space.

As to claim 8, it is inherent for the control signal in the modified figure Ting et al.'s 1C swings between the level of the input voltage and substantially double the level of the input voltage.

As to claim 9, the modified Ting et al.'s figure 1C shows that the fourth switch is turned on during a non-active status of the switching control signal, and the third switch is turned on during an active status of the switching control signal.

Allowable Subject Matter

6. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 would be allowable because the prior art fails to teach a front edge of the second clock signal is delayed by a fixed time with respect to a front edge of the first clock signal, and an active period of the second clock signal is narrower than that of the first clock signal.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

March 23, 2005